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LOW-CAPACITANCE BONDING PAD FOR SEMICONDUCTOR DEVICE

Abstract

A low capacitance semiconductor device is provided. The low capacitance semiconductor device comprises a triple well structure in the substrate, and a bonding pad structure on the substrate, wherein the substrate having a doped region of a second conductive type, a first well region of first conductive type, and a second well region of second conductive type. There is a first junction capacitance between the diffusion region and the first well region, a second junction capacitance between the first well region and the second well region, and a third capacitance between the second well region and the substrate. The first junction capacitance, second junction capacitance, the third junction capacitance and the total equivalent capacitance are coupled in series, such that the total parasitic capacitance is effectively reduced.